Paper No. 16

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte GANESH SUBRAMANIYAM and GARY HAMMOND

Appeal No. 2005-0203
Application No. 09/669,034

ON BRIEF

Before THOMAS, HAIRSTON, and NAPPI, Administrative Patent Judges.

HAIRSTON, Administrative Patent Judge.

DECISION ON APPEAL

This is an appeal from the final rejection of claims 1 through 24. In an Amendment After Final (paper number 8), claims 1, 8, 9, 20, 21 and 24 were amended.

The disclosed invention relates to a method and system for controlling the quantity of instructions per cycle executed by a central processing unit (CPU) based upon the temperature of the CPU.

Claim 1 is illustrative of the claimed invention, and it reads as follows:

> 1. A system comprising a central processing unit (CPU) including power management logic to enable the CPU to execute a first quantity of instructions per cycle whenever the temperature of the CPU exceeds a predetermined threshold and to execute a second quantity of instructions per cycle whenever the temperature of the CPU is below the predetermined threshold.

The references relied on by the examiner are:

McFarland	5,125,093	Jun. 23, 1992
Hetherington et al. (Hetherington)	5,978,864	Nov. 2, 1999
Shiell et al. (Shiell)	6,138,232	Oct. 24, 2000 (filed Dec. 19, 1997)

Claims 1 through 3 and 8 through 24 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Hetherington in view of Shiell.

Claims 4 through 7 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Hetherington in view of Shiell and McFarland.

Reference is made to the brief and the answer for the respective positions of the appellants and the examiner.

OPINION

We have carefully considered the entire record before us, and we will sustain the 35 U.S.C. § 103(a) rejections of claims 1 through 24.

We agree with the examiner's findings (answer, pages 2 and 3) that "Hetherington et al. disclose a method and system comprising a CPU 200, wherein the CPU includes power management logic 220 that enables the CPU to operate in a first execution mode (reduced at step 506) whenever the temperature of the CPU exceeds the predetermined threshold (threshold at step 502) (see col. 13, lines 44-55) and operates in a second execution mode (normal at step 510) whenever the temperature of the CPU is below the predetermined threshold (threshold at step 508) (see figures 2 and 5, col. 14, lines 5-32)."

Appellants argue (brief, pages 8 through 10) that Hetherington reduces the clock rate, as opposed to instructions per cycle, when the temperature of the processor exceeds a thermal threshold, and increases the clock rate, as opposed to instructions per cycle, when the temperature of the processor falls below the noted thermal threshold. Hetherington discloses (Figure 2; column 5, lines 20 through 31) that the clock circuit 222 that provides a clocking signal to the processor is operative to "reduce a frequency of the clocking signal to a reduced frequency" when the thermal threshold of the processor is exceeded, and is operative to "increase the frequency of the clock signal back towards a nominal frequency" when the thermal

threshold of the processor falls below a certain level. Hetherington specifically states (column 6, lines 17 through 20) that "[t]he particular examples represent implementations useful in high clock frequency operation and processors that issue and executing [sic, execute] multiple instructions per cycle ('IPC')." In other words, Hetherington teaches that instructions per cycle are indeed controlled by the frequency/rate of the clocking signal.

In sustaining a multiple reference rejection under 35 U.S.C. § 103(a), the Board may rely on one reference alone without designating it as a new ground of rejection. In re Bush, 296 F.2d 491, 496, 131 USPQ 263, 266-67 (CCPA 1961); In re Boyer, 363 F.2d 455, 458 n.2, 150 USPQ 441, 444 n.2 (CCPA 1966). Thus, the obviousness rejection of claim 1 is sustained based upon the teachings of Hetherington and the cumulative teachings of Shiell. The obviousness rejection of claims 2 through 24 is likewise sustained because appellants have chosen to let these claims stand or fall with claim 1 (brief, page 6).

DECISION

The decision of the examiner rejecting claims 1 through 24 under 35 U.S.C. § 103(a) is affirmed.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 CFR § 1.136(a).

AFFIRMED

JAMES D. THOMAS)
Administrative Patent Judge)
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KENNETH W. HAIRSTON) APPEALS AND
Administrative Patent Judge) INTERFERENCES
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